

Target Compiler Technologies, the leader in EDA tools for the design and programming of ASIPs (application-specific instruction-set processors), announced several new improvements of its Chess/Checkers tool suite geared to the design of ultra-low power SoCs. Key to the innovation is multi-faceted support for parallelism as well as RTL-level optimizations common only in the most advanced design flows. The new tool capabilities were demonstrated at the 44th Design Automation Conference in San Diego.



## Target Compiler Technologies extends processor design tools for ultra-low power multi-processor SoC design

While there is an ever growing quest for more functionality and higher performance in today's SoC designs, there is an even more pronounced need to minimize energy consumption - either to prolong battery life or to reduce operating temperatures. "Our customers tell us that following the operating frequency curve just isn't a tangible solution any more. Advanced design teams realize that they must 'get specialized' and 'go parallel' in their design approaches to meet these seemingly conflicting requirements", says Steve Cox, Target's North American VP of Business Development.

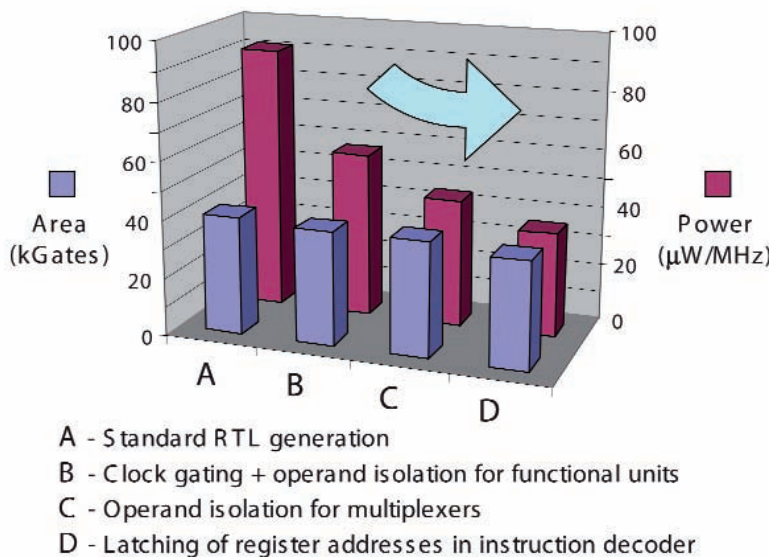
instruction-level parallelism to assure maximum computation per clock cycle. The MPSoC (multi-processor SoC) approach enables designers to target different functions to different ASIPs across the entire SoC, thereby introducing coarse-grained task-level parallelism and keeping new functionality from competing for processing cycles on the SoC's primary embedded processor. Together, the ASIP and MPSoC approaches work to minimize power dissipation overall while also maximizing computational efficiency (measured as performance/\$/watt) of a given SoC.

Optimizations have been added to the hardware generation component of the Chess/Checkers tool-suite. The new hardware generator selectively inserts dedicated logic in the ASIP's circuit to avoid unnecessary switching activity. The optimizer supports a user-controlled combination of clock gating, operand isolation, and optimized generation of register addresses. Measurements indicate that these new optimizations result in power savings of more than 60% compared to the previous Chess/Checkers release, and in power dissipation metrics that are within a few percentage points of equivalent RTL designs that were hand-optimized by low-power hardware specialists. With these optimizations, Chess/Checkers now produces the quality of results needed to effectively bridge the gap from architectural exploration to RTL implementation.

Secondly, the instruction-set simulator of the Chess/Checkers tool-suite has been extended with **new fast instruction-accurate simulation** techniques. The new simulation technology delivers a measured simulation speed of many tens of MIPS for complex DSP architectures - over 100 times faster than conventional cycle-accurate simulators. Such simulation speed is a key enabler for MPSoC designs, enabling speeds suitable for virtual prototyping, even when multiple processors are included in a single co-simulation.

Finally, **enhanced support for instruction predication** has been added to the optimizing C compiler component of the Chess/Checkers tool-suite. With instruction predication, new and more powerful

Low-power optimisations, demonstrated for an audio DSP (90 nm CMOS, clock 200 MHz)



The ASIP approach enables designers to specialize individual blocks of an SoC to their specific functional requirements - including introducing data-level and

Overall, three important new functionalities have been added to the Chess/Checkers tool-suite: First, **new low-power RTL-level opti-**

# Preface

parallelism in ASIPs is possible - unleashing greater degrees of both instruction-level parallelism (for VLIW architectures) and data-level parallelism (for SIMD architectures). SIMD architectures are common in video and image processing, as well as wireless modem applications, all of which are particularly sensitive to power concerns in this age of mobile personal devices.

*"The era of the 'power-envelope' is here. Whether targeting battery-powered devices or devices with modest thermal requirements, today's designers need tools that can meet performance requirements within a pre-defined power budget."* said Gert Goossens, CEO of Target.

*"These new capabilities add to our already well known capabilities in ASIP architectural exploration and optimization - thus extending Target's lead in ultra-low power, high performance SoC design."*

The new RTL optimizations and support for instruction predication are available in the current release of Chess/Checkers. The fast simulation capability is in beta test at customer sites now and will be released later this year. All of these new features will be made available to existing customers as a maintenance upgrade. ■

## About Target Compiler Technologies

Target Compiler Technologies is the leading provider of retargetable software tools to accelerate the design, programming and verification of application-specific processor cores (ASIPs). Target's Chess/Checkers tool suite has been applied by customers worldwide for diverse application domains, including GSM, WCDMA and HSDPA handsets, VoIP, audio coding, car infotainment, ADSL and VDSL modems, wireless LAN, hearing instruments, mobile image processing, video processing, and various control and interfacing applications. Target is a spin-off of IMEC, is headquartered in Leuven, Belgium, with North American operations in Boulder, Colorado.

## Tour de France – Tour de Technologie

Even if I am not a cyclist fanatic, I have been watching with great interest the Tour de France. In the first place, it was again one of the most demanding sport events, where the riders had to show their endurance as well in the mountains of the Alps and the Pyrenees, but also in the time trials where they just had to fight against themselves and against the clock. And although the cyclists had to ride some 3000 km, average speed in a stage was often near to or even above 50 km per hour. Cycling is not just pedaling anymore; it has become a combination of endurance, speed, team tactics and cooperation, strategy and last but not least: technology.

A lot of the achievements have been made possible thanks to the most modern technologies – to the good but also to the bad. Of course, modern technology has reshaped the bikes: they are aerodynamically shaped and made of ultra light composite materials (sometimes even too light: because a descent in the mountains can result in speeds close to 90 and 100 km / hour, a minimum weight is now imposed in order to avoid that the wheels just fold together...), and best technology is used for brakes and gears. And the cyclists themselves have adjusted their ideal position on the bike in wind tunnel tests.

Also modern ICT contributes: the riders are permanently connected with their team leader through wireless technology. They are wearing a tiny hearing instrument, through which they can obtain all information about the track, about the competitors and so on. And when our Belgian sprinter Tom Boonen can win another stage, it is also because his heart beat is continuously monitored, which gives him a perfect indication of his physical limits. Further monitoring of all kinds of body parameters can improve the optimization of the performance of endurance athletes, and ICT can bring the data on-line and wirelessly to the medical staff of the team. Research programs like Human++, conducted at IMEC, will further improve this kind of monitoring technology for sports and medical purposes.

Unluckily, technology has also improved the illegal medical means for performance enhancement – the doping. And since the Tour de France is a typical endurance trial, doping can indeed give significant result improvements. But also in the case of doping, modern information and communication technology can help to keep the sports clean. Anti-doping tests become more and more performant, in detection levels but also in detection speed. And new nanotechnologies like lab-on-a-chip, can further improve the possibility to identify the cheaters.

In the battle for clean sports, and to keep the top sport events enjoyable and exciting and fair, I challenge all our best ICT engineers, to development the best anti-doping technology, and I hope that the development of the necessary test devices can keep ahead of the development of new doping products and mechanisms.

Vive le vélo!  
Peter Simkens

Peter Simkens  
Managing Director  
DSP Valley

