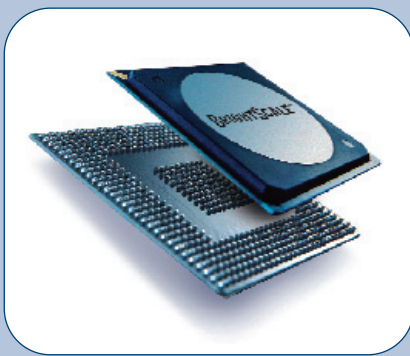




Target Compiler Technologies, the leader in customized-processor design tools, and BrightScale Inc. announced that BrightScale has selected Target's Chess/Checkers tool-suite to build a comprehensive software development toolkit for the highly parallel BrightScale Array media processing engine. The SDK includes Target's patented optimizing C-compiler, providing BrightScale's customers with the ability to adapt their end products to evolving video processing algorithms and digital television standards. The programmability enabled by the Target tools allows BrightScale's customers to support multiple functional personalities (e.g. H.264, VC-1, and MPEG2) with a single product design.

## BrightScale adopts Target's retargetable C compiler for its programmable media processor



### BrightScale Array™ can now be efficiently programmed using C

"While programmable solutions are available from other vendors today, none even come close to the performance, cost and power characteristics of hard-coded ASICs. Yet, the quickly evolving digital TV market screams out for programmability. With the impressive efficiency of Target's tools, we were able to build a video processing architecture that competes with hard-coded solutions while preserving programmability," said Dave Corbin, BrightScale's CEO. "The programmability enabled by Target's unique C compiler technology, in combination with their fast instruction-set simulation and on-chip debugging solution, delivers a powerful development environment and unsurpassed flexibility for product differentiation."

BrightScale's patented architecture is a variant of the 'Processor-in-Memory' architectures in development at major semiconductor houses worldwide. At its root, the array is a SIMD-like architecture composed

of thousands of RISC-like processing elements combined with local memory all on one chip.

BrightScale's latest product - the BA 1024 - supports dual MPEG2 transport streams and simultaneous decoding of dual HD H.264, VC-1 and MPEG2 video, while leaving enough processing headroom to support simultaneous advanced signal pre- and post-processing algorithms (e.g., 3D filters and motion-compensated de-interlacing). Early estimates show the power dissipation characteristics of this device to be approximately 10mW/MegaPixel /sec.

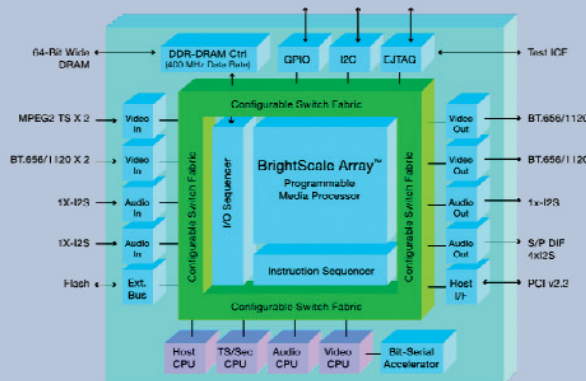
Mr. Corbin comments, "Such metrics are barely within reach of classical, hard-coded design techniques. Delivering this level of performance and efficiency with a programmable solution is clearly a breakthrough."

"We are obviously pleased with BrightScale's choice to use our tools to

create their SDK," said Gert Goossens, Target's CEO. "BrightScale is a leader in highly parallel architectures for video processing, and our retargetable optimizing C compiler assures that the parallelism available in their specialized architecture can be easily unleashed by the C programmer. With this announcement, we add efficient techniques for instruction predication to our C compiler, which are essential for both SIMD and VLIW compilation."

Target's ASIP (Application-Specific Instruction set Processor) design tools are used by engineers to design, optimize and program application-specific processor cores. They are used all the way from architectural exploration through to implementation and verification. ASIPs are primarily used in one of two ways. First, they are used to provide greater algorithmic/computational efficiency (measured as performance/\$/watt) than solutions built on standard embedded processors. Second, they are used to provide post-silicon flexibility (through programmability) to designs that might otherwise be built in hard-coded RTL. Both uses are becoming increasingly commonplace in today's SoC and FPGA designs.

BrightScale is the first North American company to announce adoption of Target's products since Target's recent expansion into the region.



All trademarks or registered trademarks mentioned in this article are the intellectual property of their respective owners.