CoolFlux DSP: An embedded ultra low power C-programmable DSP Core

PHILIPS TECHNOLOGY CAMPUS LEUVEN

TARGET

DSP Valley member Philips Digital Systems Labs Leuven (PDSL) recently completed the development of a new ultra low power DSP core, called CoolFlux DSP, now available for technology licensing. This activity runs in close cooperation with our DSP Valley partner Target Compiler Technologies, Leuven. This cooperation resulted in a high performance SW-development suite that comes with the CoolFlux core, including an optimizing C-compiler.

To develop applications for the CoolFlux, a C compiler, an assembler/disassembler, linker and debugger and a simulator are available. There is a processor-specific version of the Chess/Checkers tools from DSP Valley partner Target Compiler Technologies.

The CoolFlux DSP is an ultra low power embedded DSP 24-bit core. The core was especially developed for audio applications, including audio (de)coding, in systems with ultra low power requirements, but has a general-purpose instruction set as well. To ease the development of applications, a C compiler has been co-developed with the core. The compiler can exploit all the parallelism in the core

IMEC high-level design methodology provides substrate-noise modeling and analysis for mixed-signal systems-on-chip

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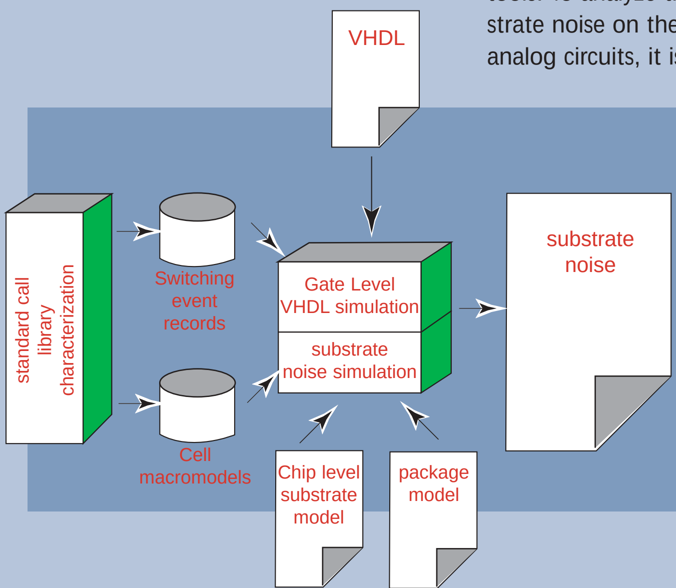
IMEC has developed a design technology supported by a prototype tool that can quickly model and then analyze noise generated on both low- and high-ohmic substrates used in ultra-deep submicron CMOS technologies. The prototype tool, called substrate-noise waveform analysis (SWAN), removes a critical barrier in the design of mixed-signal systems-on-chip by offering a means to model and analyze the substrate-noise generation which can be used in combination with existing electronic design automation (EDA) tools to determine the propagation and impact on the devices.

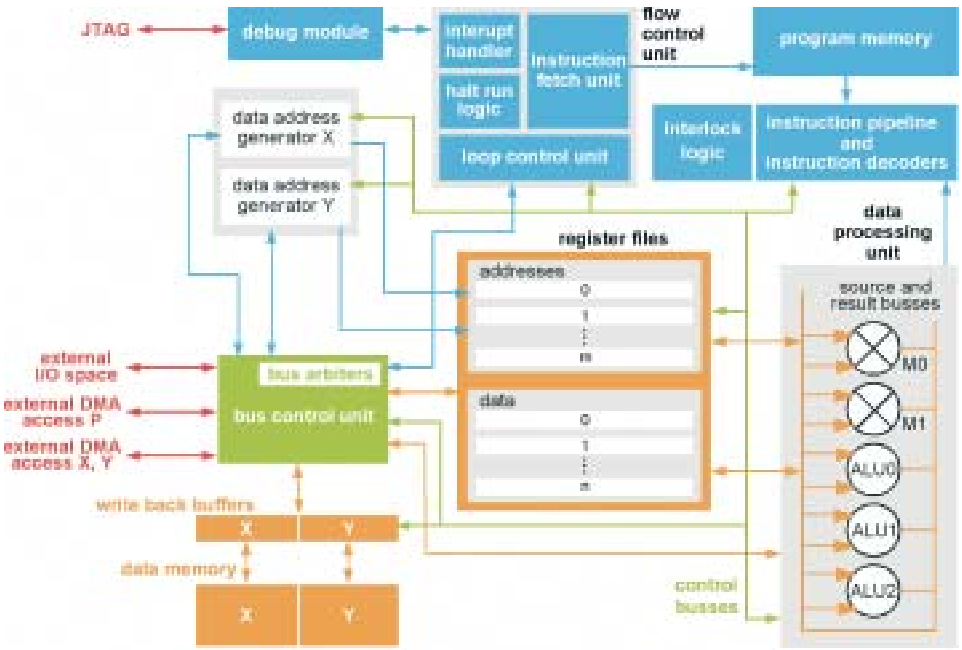
Designing mixed-signal systems-on-chip (SoCs) presents significant challenges because the noise generated by large digital circuits can severely deteriorate the performance of the analog circuits integrated on the same substrate. In addition, the complexity that can be integrated on a single die in ultra-deep submicron technologies has taxed current design methodologies and supporting EDA tools to their limits. Current available EDA tools can simulate the impact of substrate noise on analog devices but they don't help the designers in determining the substrate noise generated by the digital circuits.



IMEC's high-level substrate-noise simulation methodology for high-ohmic substrates (SWAN-HO)

IMEC's SWAN prototype tool addresses these issues by offering a complete modeling and analysis flow starting from gate-level description. The prototype tool is compatible with all commonly used industry-standard design frameworks, gate-level simulators and substrate-network extraction tools. To analyze the impact of substrate noise on the performance of the analog circuits, it is first necessary to and generates very efficient code, both from a cycle and code density perspective. Compact 32-bit instructions as well as program memory compression techniques result in small memory footprints.

CoolFlux DSP application example
As an application example, a MP3 decoder has been developed for the CoolFlux DSP. The code is developed completely in C using the compiler, without any optimizations in assembly. 14.5 MHz is required to decode a 44.1 kHz, stereo signal encoded at 128 kbps. The related memory sizes are:
P memory: 3.9 Kwords
X memory: 9.5 Kwords
Y memory: 0.4 Kwords
I/O buffers: 2.8 Kwords
This results in an estimated power consumption of less than 1 mW in CMOS18.



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CoolFlux DSP Product Features
- >1000 MOPS
- 43 kgates
- >125 MHz at 1.8 V in CMOS18 (WCMIL)
- Very efficient C-compiler, bit and cycle true instruction set simulator, linker and assembler available
- Highly efficient stack support
- Dual Harvard architecture
- A full 24-bit data path, 24x24-bit multipliers and 56-bit accumulators and ALUs
- Two multipliers, three ALUs and two saturate and truncation units are available: X multiplier: signed/signed, signed/unsigned, unsigned/unsigned Y multiplier: signed/signed
- Standard ALU operations
- Capable of addressing 64 Kwords in X, Y and P memory spaces: the program memory P consists of 32-bit words, the data memories X and Y consist of 24-bit words.
- Extensive addressing modes with modulo protection option and availability of stack pointer
- The core is fully interruptible, three interrupts are available
- Four nested loops are supported in hardware
- Extensive stop/restart instructions
- Full DMA capabilities available for both program and data memory spaces
- 64 Kbytes I/O space with support for registers and SRAM
- JTAG-based hardware debug unit (optional)

determine the amount of noise generated by the digital circuitry of the device. SWAN uses macro-models to accomplish this. The technique, which has also been used by IMEC in low-ohmic devices, has been adapted for high-ohmic substrates, including the process for addressing circuit-to-substrate coupling.
SWAN consists of two parts:
a standard-cell library characterization and a substrate-noise waveform computation. First, the substrate-noise generation and power-supply current related to switching activity of all standard cells in the design are extracted and recorded in a database together with a one-port model of the standard cell's power-supply admittance. This step needs to be done only once for a given technology and cell library. Next, the substrate noise is calculated for the design. All switching events for each gate are extracted from a standard gate-level VHDL simulation. By combining the switching-noise generation model of each gate with the switching-activity data, it is possible to calculate an accurate waveform of the switching current and ground bounce.
The switching currents can be combined with package parasitic models and, for high-ohmic substrates, with a circuit-level substrate network that has been extracted with industry-standard EDA tools and that models the circuit-to-substrate coupling.
Designers can then calculate high-ohmic substrate-noise voltages on the sensitive analog nodes caused by the ground bounce of complex digital circuits.
The design technology supported by the prototype SWAN tool is available for industry via joint research projects either bilateral or within IMEC's industrial affiliation program (IIAP) on broadband wireless systems. These projects can give partners a better insight in the mechanisms of noise generation, and hence help to develop noise-avoidance or noise-reduction techniques in mixed-signal designs.
Partners can use the modeling techniques in their own design flow to improve their productivity of mixed-signal chips (towards a first-time-right design flow).
IMEC is also looking at opportunities to launch the design technology through an EDA company for a broader public.