

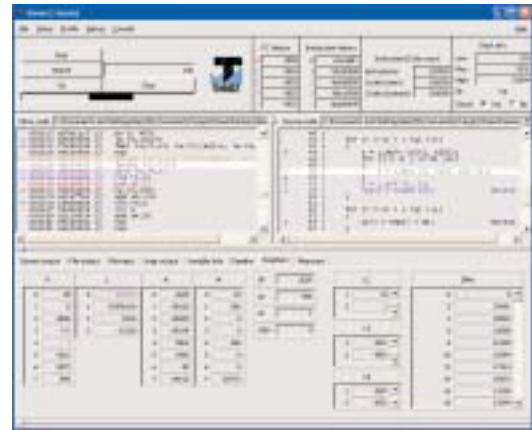


Target introduces retargetable verification and on-chip debugging for flexible IP cores in Chess/Checkers

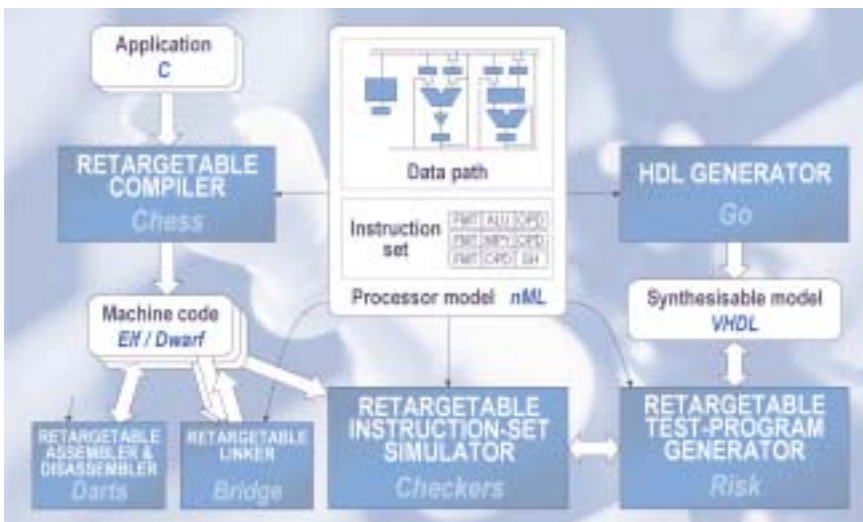
Target Compiler Technologies announces a new retargetable tool-flow for the verification of IP cores and its newly introduced on-chip debugging capabilities.

Since its spin-off from the Belgian microelectronics research center IMEC, mid 1996, Target Compiler Technologies has quickly established a leading position in the supply of retargetable tool-suites for designing and programming flexible IP cores. Its flagship product Chess/Checkers provides optimizing C compiler, an assembler/disassembler, a linker, an instruction-set simulator (ISS) with source-level debugging capabilities, and an automatic hardware description language (HDL) generator. All tools are retargetable, based on the processor description language nML.

been added to the Chess/Checkers tool-suite. This new tool, called RISK, analyses the nML processor description and automatically generates assembly-level test programs with high fault coverage for the target processor. The generated test programs can be loaded and executed both in the ISS and in the generated HDL model of the processor. Automatic comparison of ISS and HDL simulation results is provided. Secondly, Chess/Checkers now supports on-chip debugging of flexible processor cores. When using the HDL generator to produce a hardware



Graphical debugger of Chess/Checkers, which can connect both to an instruction-set simulator and to the processor hardware for on-chip debugging



Flow-chart of Target's Chess/Checkers tool-suite

Due to the increasing costs of silicon implementation, a processor design flow must provide support for the detection of hardware and software errors at a very early stage. To make this possible, Chess/Checkers has been extended with two important new functionalities.

First, a retargetable test-program generator for flexible processor cores has

implementation of the processor core from its nML description, a customizable on-chip debug controller can be included in the design. The debug controller interfaces with the chip's debug or JTAG port. An API is provided to connect the graphical source-level debugger that is part of the Chess/Checkers ISS, to this on-chip debug infrastructure.

'IP Designer' toolsuite bundles the complete offering of Target. IP Designer comprises the following retargetable tools: Chess compiler, Checkers instruction set simulator, Darts assembler/disassembler, Bridge linker, Go hardware generation, on-chip debugging and Risk verification.

"IP Designer is a product name that very well describes the essence of what we provide as a company", said Tony Picard, newly hired Sales & Marketing Manager at Target. "We offer a retargetable toolsuite that accelerates the design, the programming and the verification of flexible IP cores, in the form of programmable ASICs and embedded processors".

IP Designer has been applied successfully to design customized cores for diverse application domains, including GSM, 3G, VoIP, audio coding, ADSL, VDSL, wireless LAN, hearing aids, and various control and interfacing applications.

